

CLAIMS

1. A method for processing low voltage threshold transistors on a semiconductor wafer, the method comprising:
 - forming core transistors with drains on the semiconductor wafer;
 - forming low voltage threshold transistors with drains on the semiconductor wafer;
 - forming input/output transistors with drains on the semiconductor wafer;
 - forming a spacing layer over the core, low voltage and input/output transistors;
 - forming a first photoresist mask layer over the low voltage transistors;
 - doping the drains of the core and the input/output transistors, wherein the doping is a medium doping;
 - forming a second photoresist mask layer over the input/output transistors; and
 - doping the drains of the core and the low voltage threshold transistors, wherein the doping is a medium doping.
2. The method of claim 1 wherein the doping includes doping Arsenic.
3. The method of claim 2 wherein the doping includes doping at a range from 1 - 40 keV at 2×10^{14} to 3×10^{15} .
4. The method of claim 1 wherein the doping includes doping Phosphorus.
5. The method of claim 4 wherein the doping includes doping at a range from 1 - 30 keV 2×10^{14} to 3×10^{15} .
6. The method of claim 1 wherein the doping includes doping Boron.
7. The method of claim 6 wherein the doping includes doping at a range from 0.5 eV 2×10^{14} to 3×10^{15} .
8. The method of claim 1 wherein the doping includes doping Boron di-fluoride.
9. The method of claim 8 wherein the doping includes doping at a range from 2 keV to 20 keV 2×10^{14} to 3×10^{15} .

10. A method for processing low voltage threshold transistors on a semiconductor wafer, the method comprising:

- forming core transistors with drains on the semiconductor wafer;
- forming low voltage threshold transistors with drains on the semiconductor wafer;
- forming input/output transistors with drains on the semiconductor wafer;
- forming a first photoresist mask layer over the low voltage and the input/output transistors;
- doping the drains of the core transistors, wherein the doping is a medium doping;
- forming a spacing layer over the core, low voltage and input/output transistors;
- forming a second photoresist mask layer over the input/output transistors;
- doping the drains of the core and the low voltage threshold transistors, wherein the doping is a medium doping;
- forming a third photoresist mask layer over the core and the low voltage transistors; and
- doping the drains of the input/output transistors, wherein the doping is a medium doping.

11. The method of claim 10 wherein the doping includes doping Arsenic.

12. The method of claim 11 wherein the doping includes doping at a range from 1 - 40 keV at 2×10^{14} to 3×10^{15} .

13. The method of claim 10 wherein the doping includes doping Phosphorus.

14. The method of claim 13 wherein the doping includes doping at a range from 1 - 30 keV 2×10^{14} to 3×10^{15} .

15. The method of claim 10 wherein the doping includes doping Boron.

16. The method of claim 15 wherein the doping includes doping at a range from 0.5 eV 2×10^{14} to 3×10^{15} .

17. The method of claim 10 wherein the doping includes doping Boron di-fluoride.

18. The method of claim 17 wherein the doping includes doping at a range from 2 keV to 20 keV 2×10^{14} to 3×10^{15} .

19. A method for processing low voltage threshold transistors on a semiconductor wafer, the method comprising:

- forming core transistors with drains on the semiconductor wafer;
- forming low voltage threshold transistors with drains on the semiconductor wafer;
- forming input/output transistors with drains on the semiconductor wafer;
- forming a spacing layer over the core, low voltage and input/output transistors;
- forming a photoresist mask layer over the low voltage transistors and the IO transistors;
- doping the drains of the core transistors, wherein the doping is a medium doping;
- removing the photoresist mask layer; and
- doping the drains of the core, the low voltage threshold, and the IO transistors, wherein the doping is a medium doping.

20. The method of claim 19 wherein the doping includes doping Arsenic.

21. The method of claim 20 wherein the doping includes doping at a range from 1 - 40 keV at 2×10^{14} to 3×10^{15} .

22. The method of claim 19 wherein the doping includes doping Phosphorus.

23. The method of claim 22 wherein the doping includes doping at a range from 1 - 30 keV 2×10^{14} to 3×10^{15} .

24. The method of claim 19 wherein the doping includes doping Boron.

25. The method of claim 24 wherein the doping includes doping at a range from 0.5 eV 2×10^{14} to 3×10^{15} .

26. The method of claim 19 wherein the doping includes doping Boron di-fluoride.

27. The method of claim 26 wherein the doping includes doping at a range from 2 keV to 20 keV 2×10^{14} to 3×10^{15} .